## CLAIMS

What is claimed:

1. A method, comprising:

providing a microelectronic device including an integrated circuit mounted to a substrate;

providing a break through conductive layers of the substrate corresponding to a break in power planes of the integrated circuit;

conducting burn-in on a first portion of the integrated circuit while a second portion of the integrated circuit remains unpowered; and

conducting burn-in on the second portion of the integrated circuit while the first portion of the integrated circuit remains unpowered.

2. The method of Claim 1 wherein providing the microelectronic device including the integrated circuit mounted to the substrate further comprises providing an integrated circuit with a dual core design.

3. The method of Claim 2 wherein providing the integrated circuit with the dual core design does not affect the functioning of the integrated circuit.

4. The method of Claim 1 wherein providing the microelectronic device including the integrated circuit mounted to the substrate further comprises providing electrical connections between the integrated circuit and the substrate.

5. The method of Claim 1 wherein providing the break through the conductive layers of the substrate corresponding to the break in the power planes of the integrated circuit enables the burn-in of a first portion of the integrated circuit while a second portion of the integrated circuit remains unpowered.

6. The method of Claim 1 wherein providing the break through the conductive layers of the substrate corresponding to the break in the power planes of the integrated circuit enables the burn-in of a second portion of the integrated circuit while a first portion of the integrated circuit remains unpowered.

7. The method of Claim 1 wherein providing the break through the conductive layers of the substrate corresponding to the break in the power planes of the integrated circuit further comprises providing a first pin coupled to a first power supply to burn-in the first portion of the integrated circuit and a second pin coupled to a second power supply to burn-in the second portion of the integrated circuit.

8. The method of Claim 7 wherein providing the first pin coupled to the first power supply to burn-in the first portion of the integrated circuit and the second pin coupled to the second power supply to burn-in the second portion of the integrated circuit comprises using circuit paths which transverse the conductive layers of the substrate.

9. The method of Claim 1 further comprising heating the first portion of the integrated circuit to a burn-in temperature and implementing a test voltage.

10. The method of Claim 9 further comprising initializing the first portion of the integrated circuit.

11. The method of Claim 10 further comprising applying toggle patterns to the first portion of the integrated circuit for a designated time.

12. The method of Claim 11 further comprising powering down the first portion of the integrated circuit to burn-in the second portion of the integrated circuit.

13. The method of Claim 12 further comprising initializing the second portion of the integrated circuit.

14. The method of Claim 13 further comprising applying toggle patterns to the second portion of the integrated circuit for a designated time.

15. The method of Claim 14 further comprising powering down the second portion of the integrated circuit.

16. A system, comprising:
a microelectronic device including an integrated circuit mounted to a substrate; and a break through conductive layers of the substrate corresponding to a break in power planes of the integrated circuit, the break through the substrate and the break in the integrated circuit configured to allow rotational burn-in of the integrated circuit.

17. The system of Claim 16 wherein the integrated circuit has a dual core design that does not affect the functioning of the integrated circuit.

18. The system of Claim 16 wherein the rotational burn-in includes burn-in on a first portion of the integrated circuit while a second portion of the integrated circuit remains unpowered and burn-in on a second portion of the integrated circuit while the first portion of the integrated circuit remains unpowered.

19. The system of Claim 16 wherein a first pin coupled to a first power supply provides power to the first portion of the integrated circuit and a second pin coupled to a second power supply provides power to the second portion of the integrated circuit.

20. The system of Claim 19 wherein the first pin and the second pin use circuit paths through the conductive layers of the substrate to provide power to the first portion and the second portion of the integrated circuit.

21. A system, comprising:

a microelectronic device including an integrated circuit mounted to a substrate;

a break through multiple conductive layers of the substrate corresponding to a break in the power planes of the integrated circuit, the break in the substrate and the break in the integrated circuit dividing the microelectronic device into a first portion and a second portion; and

a first pin coupled to a first power supply to burn-in the first portion of the integrated circuit and a second pin coupled to a second power supply to burn-in the second portion of the integrated circuit.

22. The system of Claim 21 wherein the first pin and the second pin use circuit paths through the conductive layers of the substrate to provide power to the first portion and the second portion of the integrated circuit.

23. The system of Claim 21 wherein the burn-in of the first portion of the integrated circuit does not affect the second portion of the integrated circuit and the burn-in of the second portion does not affect the first portion.

24. The system of Claim 21 wherein the integrated circuit has a dual core design that does not affect the functioning of the integrated circuit.